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ANALYSIS OF AGING DETECTION ON THE EFFECTIVENESS OF RO BASED SENSOR USING VLSI

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ABSTRACT

The recycling of electronic components has become a grave problem in semiconductor industry. It is a challenge to distinguish the aged ICs from unused ones. The word 'aging' here defines the duration of IC in constant stress without interrupt. In this paper, we look at D-Wave strategies based on recycling sensors, pair of ring oscillators, which includes AQFP (Adiabatic Quantum Flux Parametric) techniques to reduce the power leakage and store the power in latches and used for next operation. The method presents the degradation detecting sensor along with testing circuitry, which performs the degradation in the threshold voltage of transistors due to increasing in the number of interface traps that occurs due to aging. The increase in threshold voltage determined by means of the frequency difference of ring oscillators. Testing functions in sensor utilized with the help of control circuitry. By applying suitable test patterns, faults present in the circuit can be identified. Thus, the reliability of the IC is greatly enhanced. Therefore, it is vital that we prevent these recycled ICs from entering critical infrastructures, aerospace, medical and defense supply chains. The proposed solutions are implemented in the 90-nm technology node. The simulation results demonstrate that our newly proposed D-Wave-aware multiple pair RO-based AQFP can detect ICs used only for a few hours.

Keywords: *Circuit aging, interface traps, AQFP (Adiabatic Quantum Flux Parametric),degradation mechanism, ring oscillator*

I.INTRODUTION

The recycling of electronic components has become a major industrial and governmental concern, as it could potentially impact the security and reliability of a wide variety of electronic systems. Nowadays aged ICs are being replaced in the market as new ICs. It affects the security and reliability of electronic systems used in various applications. The term aging represents the duration of IC in the powered ON state. An aged IC is a product which is not genuine compared to new IC for three reasons: (1) it does not have same performance as like original component, (2) the specifications of the aged ICs are unknown, and (3) unauthorized component. These aged ICs enter the market when the recyclers remove these aged ICs from the damaged board or unused board for the purpose of reselling these aged ICs on new boards.

Recycled ICs are those that are reclaimed or recovered from a used system and are then misrepresented as new components produced by an original component manufacturer. Recycled ICs generally exhibit lower performance and have shorter lifetimes compared with the authentic ones, due to the effects of aging during their prior usage and mishandling during the recycling process. The recycling process consists of aggressively removing components from printed circuit boards under very high temperatures. The components are then subjected to washing, sanding, repackaging, and remarking, all of which could damage the ICs and introduce many defects and anomalies compactable structure in proposed chip design. The electronic components pose a great risk to the security and reliability of electronic systems. Due to the global nature of the electronic component supply chain, cases of counterfeit electronics are on the rise. Counterfeit components, whether they are integrated circuits (ICs), dies or electronic systems, can be broadly classified into recycled, remarked, out-of-spec, defective, overproduced and cloned component

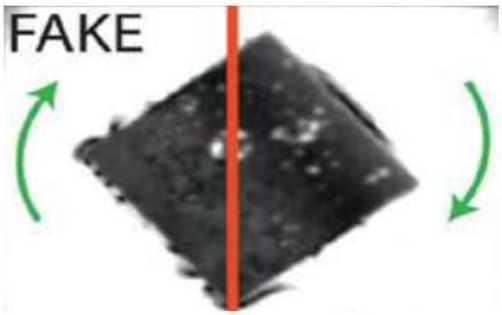

Fig 1: Fake IC

II. BACKGROUND AND RELATED WORK

A.IC Aging

Aging of an IC can be defined in terms of duration of IC in constant stress without interrupt when it is in continuous ON state. Due to increase in the number of interface traps that occurs due to aging, there will be a degradation in threshold voltage of transistor. This degradation can be detected by a sensor consist of ring oscillator which contains a chain of inverters along with control transistors [1]. Detection of degradation is performed by means of frequency difference of ring oscillator in the active mode of IC without any fault in the circuit. If there is any fault in the circuit due to aging, that can be detected by the testing circuit with suitable test patterns along with control circuitry which determines whether primary inputs enter into the circuit or the test inputs enter into the circuits. The major difference between detecting recycled ICs by physical and electrical test methods and on-chip sensors is that test methods rely on finding the defects, and anomalies present in the recycled ICs.

These test methods are extremely expensive and slow. Moreover, recycling has evolved over the last few years, and the level of sophistication in the recycling process has significantly improved [2]. It is very difficult, if not impossible to restore the degradation caused by aging in recycled ICs. A shift in circuit parameters due to aging will occur when a chip is used in the field for any period of time. when ICs have to be used in high-risk or critical applications, where recycled ICs could cause catastrophic system failures or pose a significant risk.

To address these challenges, this paper presents several different CDIR structures based on ROs. We propose a lightweight CDIR structure suitable for both large and small digital ICs. The structure itself is an RO-based sensor[3]. Our new design is NBTI-aware and exploits aging much more efficiently than the O-CDIR. We call this design as N-CDIR, where "N" stands for NBTI-aware. We propose a new N-CDIR with multiple reference and stressed RO-pairs.

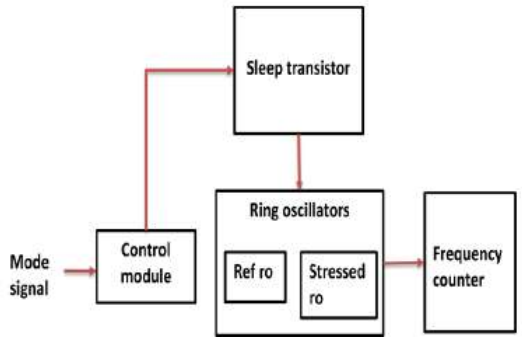

Fig 2: RO block diagram

Support vector machines (SVM) aging analysis for FPGAs using ring oscillators and path-delay fingerprinting have also been suggested to detect counterfeit ICs. Techniques such as hardware metering ICs once they are produced in the boundry and require authentication from the design house, so that only authenticated chips can be accepted. dynamic current analysis to determine the aging difference between high-activity and low activity portions of functional blocks[4]. An approach requires at least a year of aging for reliable results. Thus, there is a need for design-for-anti-counterfeiting (DfAC) strategies that incorporate self-sufficient anti-counterfeiting mechanisms into chips during the design phase, with minimal overhead. the use of on-chip sensors based on ring oscillators (ROs) for detecting recycled die and ICs which measures the difference between the frequencies of a stressed RO, designed to age rapidly, and a reference RO. CDIR (Combating Die and IC Recycling) sensors, which are designed to account for negative bias temperature instability (NBTI) [5]. silicon odometer sensors are specifically designed to monitor IC aging phenomena and are not geared towards the detection of recycled ICs.

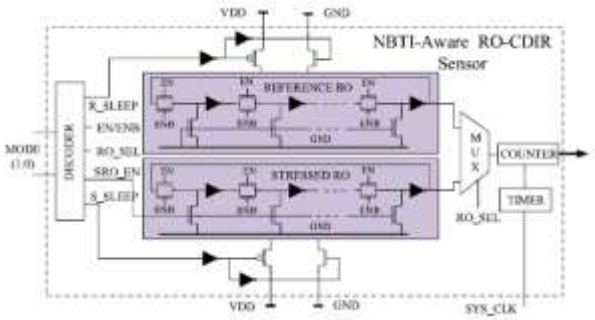

Fig 3: Architecture of N-CDIR sensor

B. ARCHITECTURE OF N-CDIR

The stressed RO is modified in such a way that all the inverters are stressed constantly. To achieve this, we have introduced a pass transistor in between every pair of inverters. The inputs of all the inverters are pulled down to ground using an nMOS network[6]. We have mimicked the stressed RO' structure in the reference RO in order to match all the internal parameters (node capacitance, resistance, and so on). This is to

ensure that at time 0, when there is no aging, the difference between the two ROs is minimal and is mainly impacted by the small variations present between the two ROs.

The DECODER generates all the internal signals for a specific mode. When EN = 0, both ROs oscillate while the sleep transistors are ON. The signals *EN* and *SRO_EN* can never be 1 simultaneously as this would create a short circuit in the design. Like O-CDIR, the COUNTER measures the cycle count of the two ROs during measurement, which is controlled by the TIMER. There are four distinct modes of operation.In manufacturing and burn-in tests (MODE = 00), our objective is to protect both ROs from aging. In this mode, both ROs enter in sleep mode by being cut off from the power and ground line. R_SLEEP and S_SLEEP will be assigned to 0 during this entire operation. In normal operation (MODE = 01), the reference RO will remain in the sleep mode while the stressed RO will be in the stressed mode[7]. All the inverters in the stressed RO will be given a dc stress by pulling their inputs to ground. In authentication mode (MODE = 10 or 11), the reference RO will be activated to measure its frequency, which should correspond to the RO frequency of the new IC at time 0. Then, the stressed RO will be activated by setting *SRO_EN* to 0, and its degraded frequency will be measured.

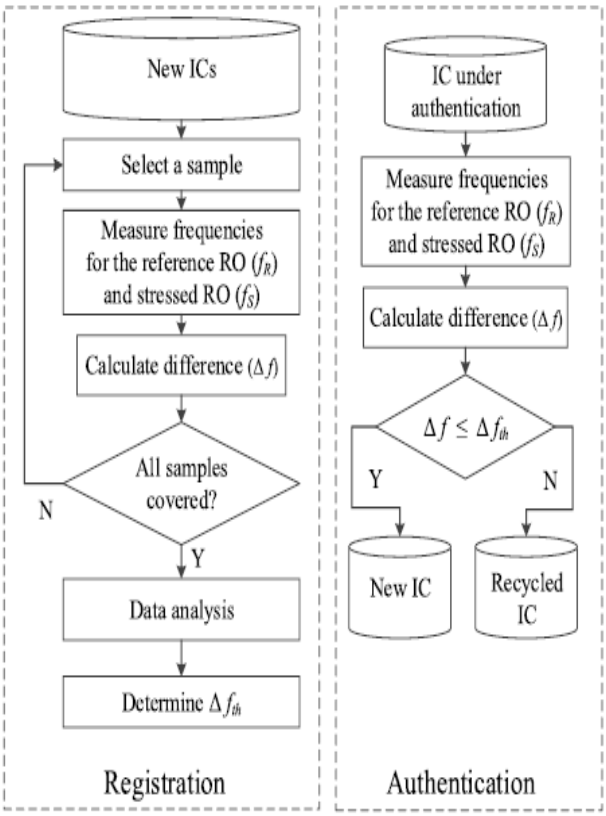

Fig. 4. Registration and authentication flow for N-CDIR

III. PROPOSED WORK

Adiabatic Quantum-Flux-Parametron (AQFP) logic is one of the energy-efficient superconductor logics.We designed and implemented several AQFP logic circuits [8], including a majority gate and a full adder. In addition, we proposed and designed the quantum-flux-latch (QFL) [9], [10] as a novel latch for AQFP logic to achieve practical energy efficient computing systems using AQFP logic.

A. QUANTUM-FLUX-LATCH

Fig. 5 shows a circuit schematic of a quantum-flux-latch (QFL), which is composed of an AQFP gate, the input inductance of which is replaced by a storage loop. The storage loop includes a Josephson junction,

*J*0, and is biased by the dc current, *I*b. The internal state of a QFL is represented by the absence or presence of a single-flux-quantum (SFQ) stored in the storage loop. The read gate, which is driven by an excitation current, *I*x, can non-destructively read out the internal state. The flux state in the storage loop changes only when an SFQ is stored or escapes.When both of the write gates are in logic state "1", *J*0 switches, and the storage loop stores an SFQ, which corresponds to "Write 1". When both of the write gates are in logic state "0", the stored SFQ escapes from the loop, which corresponds to "Write 0".

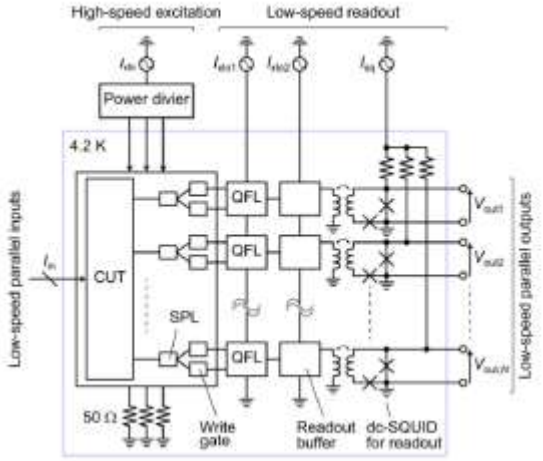

Fig.5. Block diagram of a QFL

When the two write gates are in the different logic states, the QFL holds its current state, because the applied fluxes from the write gates cancel each other. A QF is composed of only three junctions and requires only one clock cycle for both read and write. We reported an experimental demonstration of a QFL and a 1-bit shift register using QFLs.

B.QFL-BASED HIGH-SPEED TEST CIRCUIT

To demonstrate the AQFP circuit at high speed (in the GHzrange), we use QFLs to hold and read out data. A QFL-based high-speed test circuit (QHTC),where circuits under test (CUTs) are driven by high-speed excitation currents, *I*xhi, and the QFLs and readout buffers are driven by low-speed excitation currents, *I*xlo1 and xlo2, respectively.Three-phase high-speed excitation currents, *I*xhi1, *I*xhi2,and *I*xhi3, are generated using a power divider, which also adds dc-offset to each excitation current, and are terminated by on chip 50 Ω resistances. Before the QFLs are driven by *I*xlo1, low-speed inputs are fixed and the output data of the CUTs are stored in storage loops of the QFLs after split by splitter (SPL) gates. Although the CUTs switch at every cycle of the high-speed excitation currents, the stored data can be latched by QFLs when *I*xlo1 rises without timing synchronization between the low-speed inputs and the high-speed excitation currents. The latched data are read out at low speed using dc-SQUIDs, where we inserted the readout buffers to reduce back actions from the dc-SQUIDs to the QFLs.

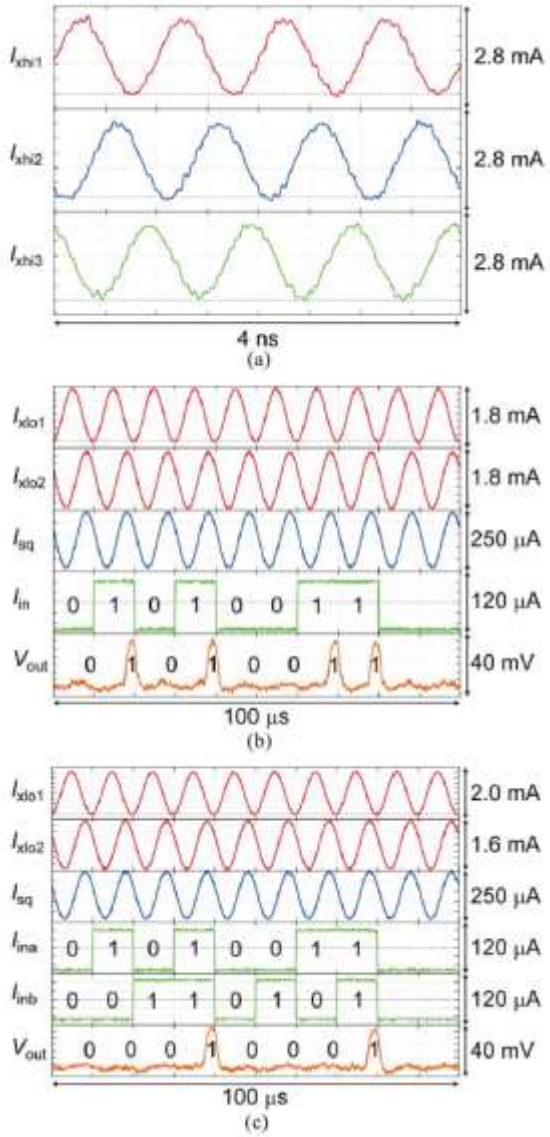

Fig. 6. High-speed measurement results at 1 GHz. (a)

Three-phase excitation currents at 1 GHz generated by

a power divider. (b) α: the CUT is a buffer gate. (c) γ:

the CUT is an AND gate.

CONCLUSION

We proposed the QHTC as a high-speed test circuit with D-Wave-aware of AQFP logic gates, to test the aging ICs, where the output data of CUTs, operating at high speed, are stored in QFLs and are read out at low speed. We experimentally demonstrated high-speed operation of AQFP buffer gates and AND gates at 1 GHz. Obtained margins of high-speed and 90-nm technology the excitation currents were more than ±30%, which is wide enough for practical systems using AQFP logic gates. The margin of the dc bias currents to QFLs was smaller than expected but increased to ±16% by reducing the size of the junctions in QFLs.

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